

Abstract

A multi-mode predictor for a processor having a plurality of prediction modes is disclosed. The prediction modes are used to predict non-binary values. The predictor is a multi-mode predictor comprising a per-IP (“PIP”) table and a next value table. The PIP table includes a plurality of PIP information fields and the next value table includes a plurality of fields. The multi-mode predictor also includes a plurality of prediction modes. The processor includes a set of instructions that index the PIP table to provide a valid signal. The processor also includes a set of predicted values for the set of instructions. The set of predicted values is stored in the PIP table and the next value table. According to the valid signal a hit/miss condition in the next value table, a predicted value is selected from the PIP table or the next value table.